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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/784,873	02/24/2004	Eiji Taguchi	65933-072	8297

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EXAMINER	
SHERMAN, STEPHEN G	

ART UNIT	PAPER NUMBER
2629	

DATE MAILED: 12/05/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/784,873	TAGUCHI ET AL.	
	Examiner	Art Unit	
	Stephen G. Sherman	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 February 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *24 February 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

3. Claims 1-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kubota et al. (US 6,067,066) in view of Copley et al. (US 2002/0063646).

Regarding claim 1, Kubota et al. disclose a signal line drive circuit, including:

a high-voltage side switch block and a low-voltage side switch block (Figure 29 shows the high-voltage side switch block containing switches TOA1 through TOA8, and low-voltage side switch block containing switches TOB1 through TOB8.);

a ladder resistor across which a high-voltage side voltage and a low-voltage side voltage are applied through a high-voltage side selection switch selected from said high-voltage side switch block and a low-voltage side selection switch selected from said low-voltage side switch block, respectively (Figures 29 and 30 show that that ladder resistor containing resistors R1 through R8 receives a high side voltage VA from one of the high-voltage side switches TOA1 through TOA8 and also receives a low-side voltage VB from one of the low-voltage side switches TOB1 through TOB8.); and

a plurality of intermediate voltage takeout signal lines which take out a first intermediate voltage from an end point, connected to the high-voltage side selection switch, of said ladder resistor and which then take out a second and a third, ... and (k-1)th intermediate voltage from any other end points thereof in the order of closeness to the high-voltage side selection switch and which take out a kth intermediate voltage from an end point, connected to the low-voltage side selection switch, of said ladder resistor, where k is an integer greater than or equal to 2 (Figure 30 shows a plurality of intermediate voltage takeout signal lines VI1 through VI8 which are connected starting at an end point from the high voltage side of the ladder network receiving VA and ending at the low-voltage side of the ladder network receiving VB.).

Kubota et al. fail to teach wherein a dividing resistance value which causes a difference between the first intermediate voltage and the second intermediate voltage among resistance components in said ladder resistor is greater than an on-resistance value of the high-voltage side selection switch.

Copley et al. disclose wherein an on-resistance value of a switch is much smaller than the value of the individual resistors to which it is coupled (Paragraph [0053]).

Therefore it would have been obvious to "one of ordinary skill" in the art at the time the invention was made to make the on-resistance value of the switches on the high-voltage side as taught by Kubota et al. have a lower resistance value than the resistors as taught by Copley et al. because making transistors with very small resistance values allows for higher speed driving, and then making the on-resistance values of all of the switches being then smaller than the resistance values of the individual resistors such that the ratio of voltages is kept allows for the output to be more precisely rationed over temperature and supply variations.

Regarding claim 2, please refer to the rejection of claim 1, and furthermore since as stated above the resistance values of the different resistors in the string are the same, the combination of Kubota et al. and Copley et al. would also teach wherein a dividing resistance value which causes a difference between the (k-1)th intermediate voltage and the kth intermediate voltage among resistance components in said ladder resistor is greater than an on-resistance value of the high-voltage side selection switch.

Regarding claim 3, please refer to the rejection of claim 1, and furthermore since as stated above the on-resistance values of the different switches as made to be the same, the combination of Kubota et al. and Copley et al. would also teach wherein the signal line drive circuit is structured such that a relationship of a potential difference

between the high-voltage side voltage and a predetermined reference voltage and that between the low-voltage side voltage and the reference voltage and a relationship of on-resistance values of said high-voltage side and low-voltage side switches are reversed, because if the values are the same then the value can be reversed and a difference will not be realized.

Regarding claim 4, disclose a signal line drive circuit according to Claim 1.

Kubota et al. also disclose a signal line drive circuit including:

an upper selection circuit which receives an input of x bits out of n-bit image signals and selects the high-voltage side selection switch and the low-voltage side selection switch from said high-voltage side switch block and said low-voltage side switch block, respectively, where n is an integer greater than or equal to 2 and x is an integer greater than or equal to 1 and less than n (Figure 29 shows the upper selection circuit 33, which receives only part of a signal at a time such that only two switches, each one corresponding to one of the switches from either TOA1-TOA8 or TOB1-TOB8, in order to out a selected voltage for the high-voltage side VA and the low-voltage side VB.); and

a lower selection circuit which selects a desired intermediate voltage takeout signal line from said plurality of intermediate voltage takeout signal lines by signals of (n-x) bits, excluding the x bits, among the image signals (Figure 30 shows the selection circuit 32 which is used to select a desired intermediate voltage from the plurality of values.).

Regarding claim 5, this claim is rejected under the same rationale as claim 4.

Regarding claim 6, this claim is rejected under the same rationale as claim 4.

Regarding claim 7, disclose a signal line drive circuit according to Claim 4.

Kubota et al. also disclose wherein said upper selection circuit is such that logic to select the high-voltage side selection switch and the low-voltage selection switch exists outside the path of lines on which a plurality of switches included in said switch blocks is interposed (Figure 29 shows that the selection of the switches takes place outside of the circuit 33 and the signals are input at the terminals S1 through S8.), and wherein said lower selection circuit is such that at least part of logic to select a desired one of said plurality of intermediate voltage takeout signal lines is interposed on the path of said plurality of intermediate voltage takeout signal lines (Figure 30 shows that the switches G1-G8, which are at least part of the logic to select the switches, as located in the path of the takeout signal lines VI1-VI8.).

Regarding claim 8, this claim is rejected under the same rationale as claim 7.

Regarding claim 9, this claim is rejected under the same rationale as claim 7.

Conclusion

4. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Yoshida (US 2004/0075633) discloses of a data driver including a nigh voltage and low voltage side connected to a resistor string which includes a plurality of outputs (Figures 4 and 5).

Nakamura et al. (US 6,411,273) discloses of a driver circuit that comprises a resistive dividing type digital-to-analog converter circuit.

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Stephen G. Sherman whose telephone number is (571) 272-2941. The examiner can normally be reached on M-F, 8:00 a.m. - 4:30 p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amr Awad can be reached on (571) 272-7764. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

SS

16 November 2006

AMR A. AWAD
SUPERVISORY PATENT EXAMINER